IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
Dale E. Gulick

Serial No.: 10/005,648

Filed: December 3, 2001

For: EMBEDDED PROCESSOR SUPPORTING BOTH ACPI AND ASF OPERATIONS

Customer No. 8012

Examiner: Thomas J. Cleary

Group Art Unit: 2111

Att'y Docket: 2000.051600

Customer No. 26290

RESPONSE TO NOTIFICATION OF NON-COMPLIANT APPEAL BRIEF MAILED AUGUST 7, 2009

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This paper is submitted in response to the Notification of Non-Compliant Appeal Brief dated August 7, 2009 for which the one-month date for response is September 7, 2009. This paper is being electronically filed on September 4, 2009, therefore it is timely filed.

No fees are believed to be due in connection with this response. However, should any fees be required under 37 C.F.R. §§ 1.16 to 1.21, the Director is authorized to deduct such fees from **Williams, Morgan & Amerson's P.C. Deposit Account 50-0786/2000.051600.**

Enclosed herewith is a "revised" Claims Appendix. The "revised" Claims Appendix includes the correct copy of the appealed claims. It is believed that the "revised" Claims Appendix submitted herewith overcomes all of the deficiencies noted in the August 7, 2009 Notice received from the Office.

Please feel free to contact the undersigned to the extent any further information is required or if there are any other questions.

Date: September 4, 2009

Respectfully submitted,

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CLAIMS APPENDIX

1. A microcontroller configurable as either an Alert Standard Format master or an Alert Standard Format slave, wherein the microcontroller is configured as either the Alert Standard Format master or the Alert Standard Format slave, wherein the microcontroller is further configured as an Advanced Configuration and Power Interface controller.

2. The microcontroller of claim 1, configured as the Alert Standard Format master.

3. The microcontroller of claim 2, wherein the microcontroller is coupled to an SMBus, and the microcontroller is further configured to receive Alert Standard Format status data from Alert Standard Format devices over the SMBus.

4. The microcontroller of claim 1, configured as the Alert Standard Format slave.

5. The microcontroller of claim 4, wherein the microcontroller is configured to receive status data from one or more Alert Standard Format devices, wherein the microcontroller is further configured to forward the status data from the one or more Alert Standard Format devices to the Alert Standard Format master.

6. The microcontroller of claim 1, further configured as an embedded 8051 microcontroller.

7. The microcontroller of claim 1, comprised in a bridge.

8. The microcontroller of claim 7, wherein the bridge is a south bridge.

9. An integrated circuit, comprising:

an internal bus; and

a microcontroller connected to the internal bus, wherein the microcontroller is configured to master the internal bus, wherein the microcontroller is configurable as either an Alert Standard Format (ASF) master or an ASF slave, wherein the microcontroller is configured as either the ASF master or the ASF slave, wherein the microcontroller is further configured as an Advanced Configuration and Power Interface (ACPI) controller.

10. The integrated circuit of claim 9, wherein the microcontroller is configured as the ASF master.

11. The integrated circuit of claim 10, wherein the microcontroller is coupled to an SMBus, wherein the microcontroller is further configured to receive ASF status data from one or more ASF devices over the SMBus.

12. The integrated circuit of claim 10, further comprising:

an Ethernet controller coupled to the internal bus, wherein the Ethernet controller and the microcontroller are configured to exchange data over the internal bus.

13. The integrated circuit of claim 12, further comprising:

a plurality of buffers coupled between the microcontroller and the Ethernet controller for buffering the data.

14. The integrated circuit of claim 13, wherein the plurality of buffers are connected between the internal bus and the Ethernet controller.

15. The integrated circuit of claim 12, and wherein the Ethernet controller is configured to route Alert Standard Format messages to the microcontroller.

16. The integrated circuit of claim 12, further comprising:

a remote management and control protocol set command unit connected to the internal bus, wherein the remote management and control protocol set command unit is configured to execute remote management and control protocol commands received from an external management server through the Ethernet controller.

17. The integrated circuit of claim 9, wherein the microcontroller is configured as the ASF slave.

18. The integrated circuit of claim 17, wherein the microcontroller is configured to receive status data from one or more ASF devices, wherein the microcontroller is further configured to forward the status data from the one or more ASF devices to a remote ASF master.

19. The integrated circuit of claim 17, further comprising:

an Ethernet controller coupled to the internal bus, wherein the Ethernet controller and the microcontroller are configured to exchange data over the internal bus.

20. The integrated circuit of claim 19, further comprising:

a plurality of buffers coupled between the microcontroller and the Ethernet controller for buffering the data.

21. The integrated circuit of claim 20, wherein the plurality of buffers are connected between the internal bus and the Ethernet controller.

22. The integrated circuit of claim 19, wherein the Ethernet controller is configured to route ASF messages to an external ASF master.

23. The integrated circuit of claim 9, wherein the microcontroller is further configured as an embedded 8051 microcontroller.

24. The integrated circuit of claim 9, wherein the integrated circuit is configured as a bridge, wherein the bridge further includes:

a first bus interface logic for coupling to a first external bus; and

a second bus interface logic for coupling to a second external bus.

25. The bridge of claim 24, wherein the bridge is configured as a south bridge.

26. The south bridge of claim 25, further comprising:

a plurality of south bridge registers; and

a register bridge connected to the internal bus, wherein the microcontroller is configured to read each of the plurality of south bridge registers through the register bride.

27. The integrated circuit of claim 9, further comprising:

a first ACPI embedded controller interface.

28. The integrated circuit of claim 27, further comprising:

a second ACPI embedded controller interface.

29. The integrated circuit of claim 28, further comprising:

a third ACPI embedded controller interface.

30. The integrated circuit of claim 9, further comprising:

an ASF status register.

31-40. (Withdrawn)

41. A computer system, comprising:

an external bus;

an integrated circuit, comprising:

an internal bus;

a microcontroller connected to the internal bus, wherein the microcontroller is configured to master the internal bus, wherein the microcontroller is configurable as either an Alert Standard Format (ASF) master or an ASF slave, wherein the microcontroller is configured as either the ASF master or the ASF slave, wherein the microcontroller is further configured as an Advanced Configuration and Power Interface (ACPI) controller; and

a bus interface logic connected to the external bus; and

a processor coupled to the external bus.

42. The computer system of claim 41, wherein the microcontroller is configured as the ASF master for the computer system.

43. The computer system of claim 42, further comprising:

an SMBus;

one or more ASF devices coupled to the SMBus; and

wherein the microcontroller is further configured to receive ASF status data from the one or more ASF devices over the SMBus.

44. The computer system of claim 42, further comprising:

an Ethernet controller coupled to the internal bus, wherein the Ethernet controller and the microcontroller are configured to exchange data over the internal bus; and

wherein the processor is configured to communicate over a network using the Ethernet controller.

45. The computer system of claim 44, and wherein the Ethernet controller is configured to route Alert Standard Format messages to the microcontroller.

46. The computer system of claim 44, further comprising:

a remote management and control protocol set command unit connected to the internal bus, wherein the remote management and control protocol set command unit is configured to execute remote management and control protocol commands received from an external management server through the Ethernet controller.

47. The computer system of claim 41, wherein the microcontroller is configured as the ASF slave.

48. The computer system of claim 47, wherein the microcontroller is configured to receive status data from one or more ASF devices, wherein the microcontroller is further configured to forward the status data from the one or more ASF devices to a remote ASF master.

49. The computer system of claim 48, further comprising:

a network interface card coupled to the integrated circuit and to the processor, wherein the network interface card is configured as the Alert Standard Format master, and

wherein the Ethernet controller is configured to route Alert Standard Format messages to the network interface card.

50. The computer system of claim 47, further comprising:

an Ethernet controller coupled to the internal bus, wherein the Ethernet controller and the microcontroller are configured to exchange data over the internal bus.

51-54. (Withdrawn)

55. A method for operating a computer system, the method comprising:

receiving an Alert Standard Format message at a microcontroller in the Alert Standard Format south bridge;

receiving an ACPI event notification at the microcontroller in the Alert Standard Format south bridge; and

causing a system management interrupt to be generated using the microcontroller in the Alert Standard Format south bridge.

56-74. (Withdrawn)

75. A south bridge, comprising:

controller means for receiving an Alert Standard Format message;

controller means for receiving an ACPI event notification; and

means for generating a system management interrupt.

76-85. (Withdrawn)